Display Interfacing

Managing the transitions and looking to the future

Jim Schuessler

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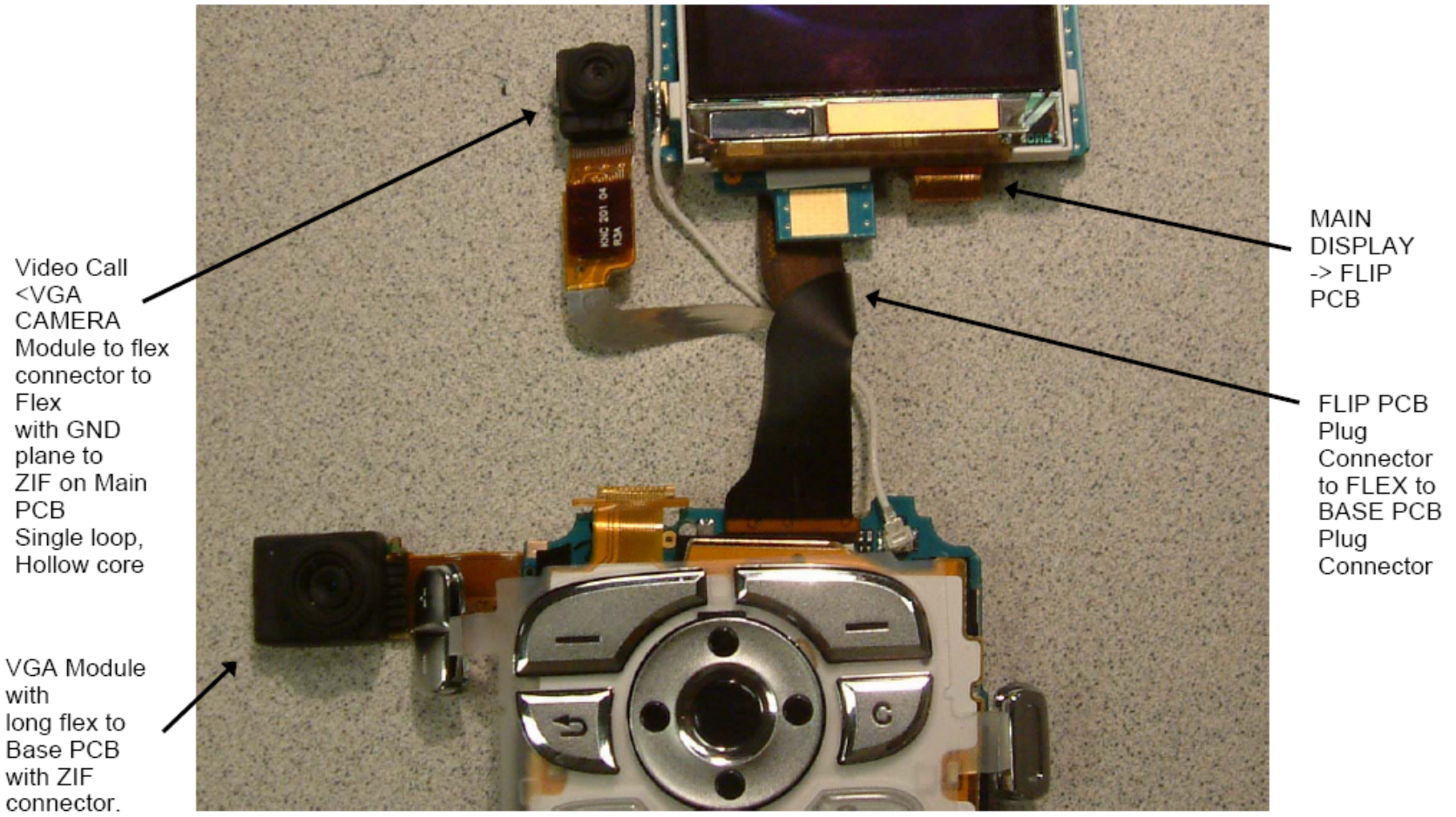
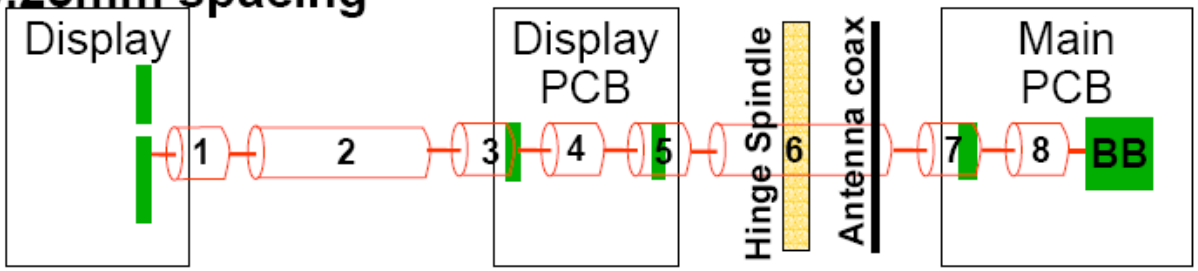
2004: Wide complex parallel interconnects



- **Sony-Ericsson Z1010 – typical of many**

Poor electrical environment

1. Dual chip COG : bump-ITO-ACF
2. 35mm flex
3. ZIF connector
4. 20mm trace FR4 2 layer 0.2mm width; 0.3mm spacing
5. ZIF connector
6. 40-50mm flex
7. Connector 0.65mm pin pitch
8. 70-80mm trace FR4 8 layer 0.08mm width; 0.25mm spacing



- **Yet, using LV-CMOS I/O, it works!**

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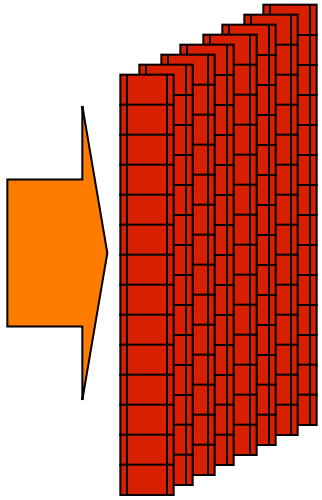
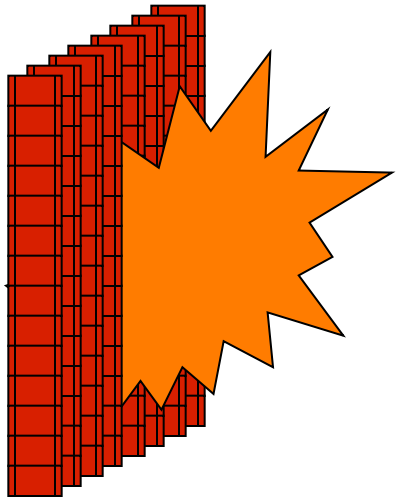
Hitting the wall

- Large number of signals
  - Large internal volume
  - Lower MTBF
  - High cost of chips, boards, cables and connectors
- Increasing power consumption
- Increasing EMI
- Longer design and system integration time



- High speed serial interconnects reduce these problems
- and… they are not just for displays!

Explosion of solutions



Company	Name	Initial Release or Specification
Intel	Mobile Scalable Link (MSL) - not for displays	Mid. 2003
National Semiconductor	Mobile Pixel Link (MPL)	Fall, 2003
NEC Electronics	Mobile CMADS	Nov., 2003
Rohm	Mobile Shrink Data Link (MSDL)	Nov., 2003
Samsung	Pseudo-diff., i-mode Mobile Bus (SiM Bus)	Mid. 2004
Seiko-Epson/Renesus	Mobile Video Interface (MVI)	Aug. 2004
Qualcomm (VESA)	Mobile Display Digital Interface (MDDI)	Mid. 2004
Nokia	Compact Display Port (CDP)	End 2004
Fairchild	MicroSERDES	Mid. 2005
Mobile Industry Processor Interface Alliance (MIPI Alliance)	Display Serial Interface (DSI), Display Command Set (DCS)	End 2005

- **Then the dust starts to settle:**
  - **Most of the GSM world coalesces around MIPI and DSI**
  - **The dominance of Qualcomm establishes MDDI in the CDMA world**

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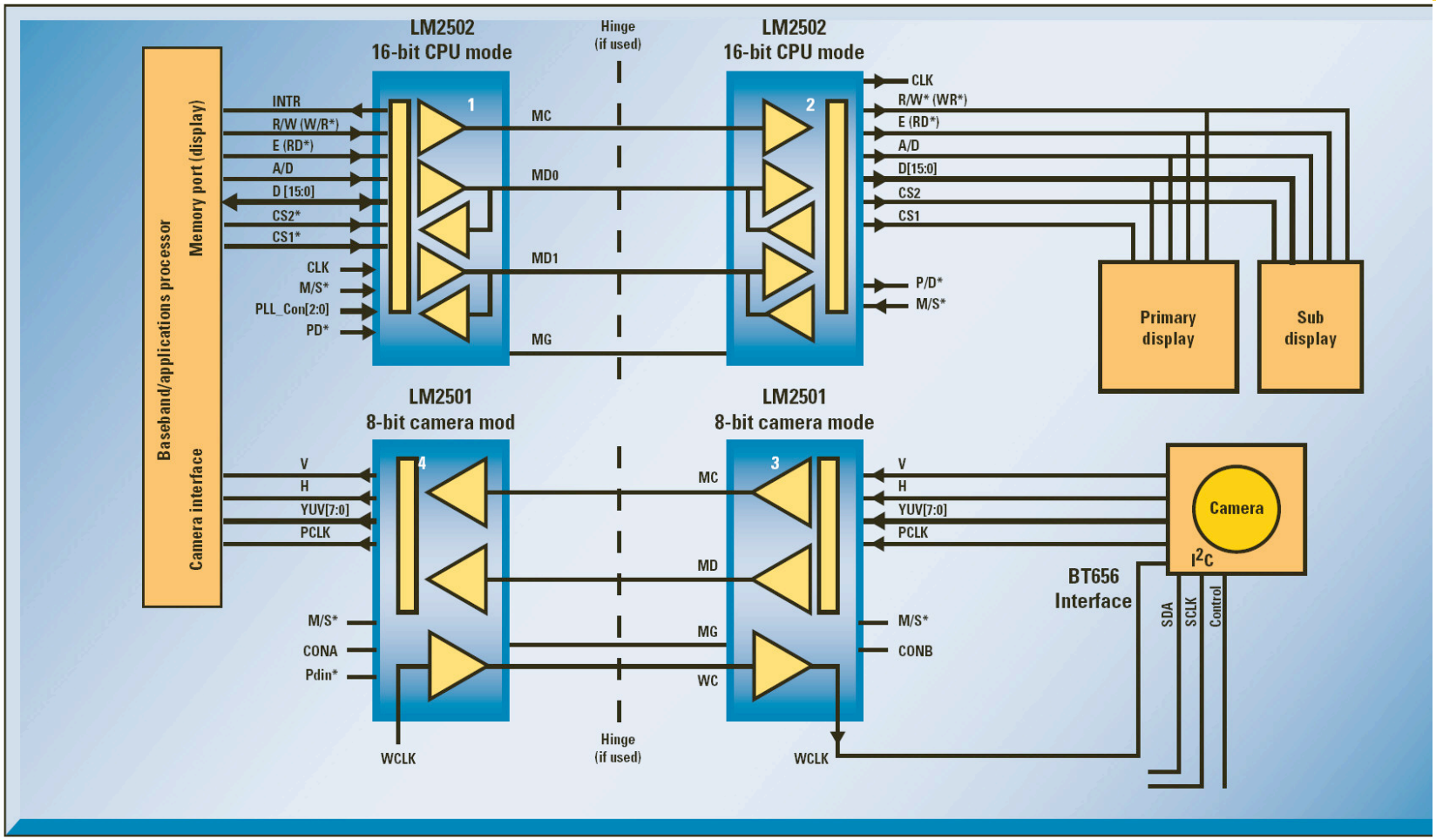
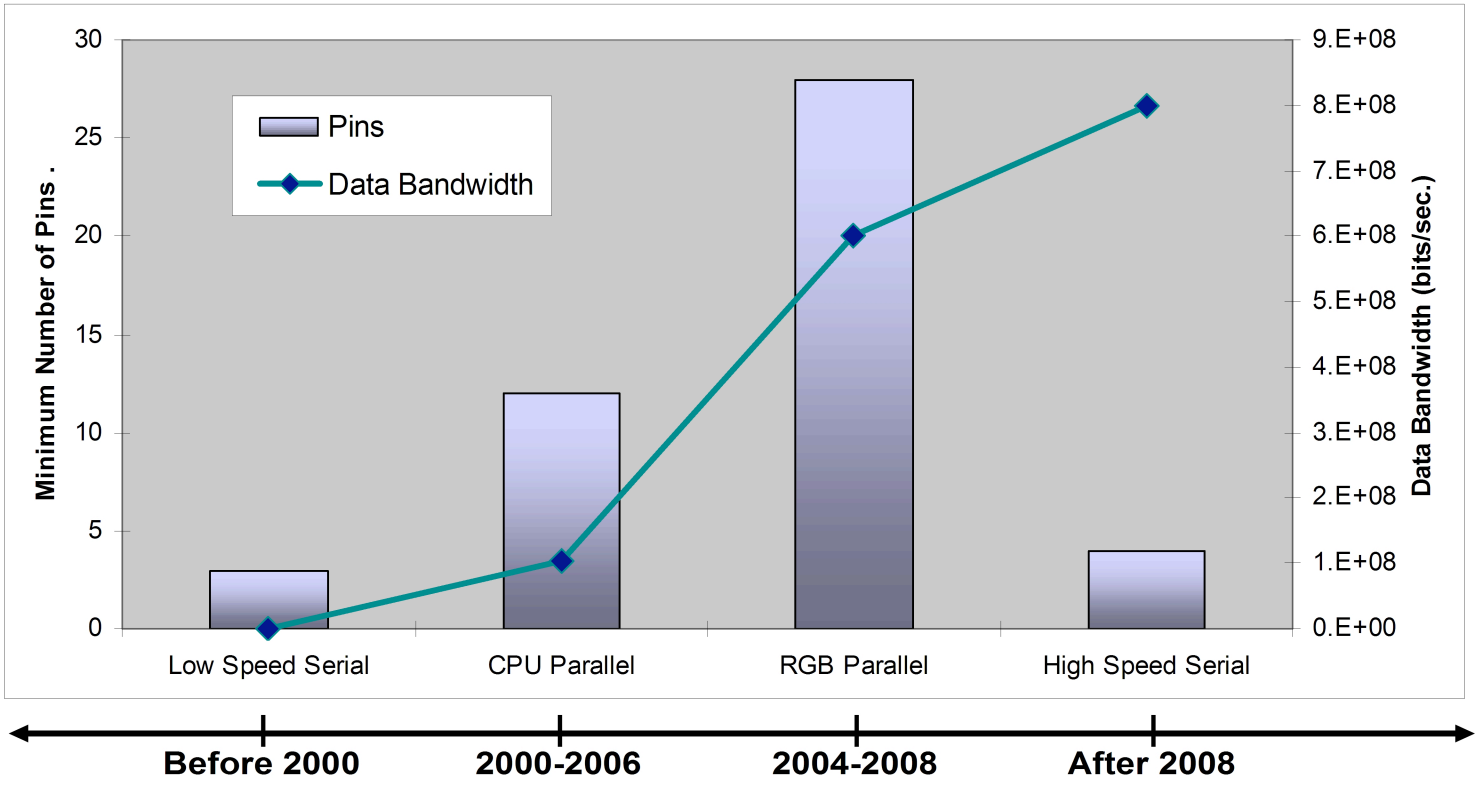
Transition: Use of translator devices



- **Early proprietary serial interface from National Semiconductor**
  - **Mobile Pixel Link**

More efficient use of pins



- **400Kbps to ~400Mbps: Three orders of magnitude speed increase**
- **3 pins to 4 pins: 25% increase in pins**

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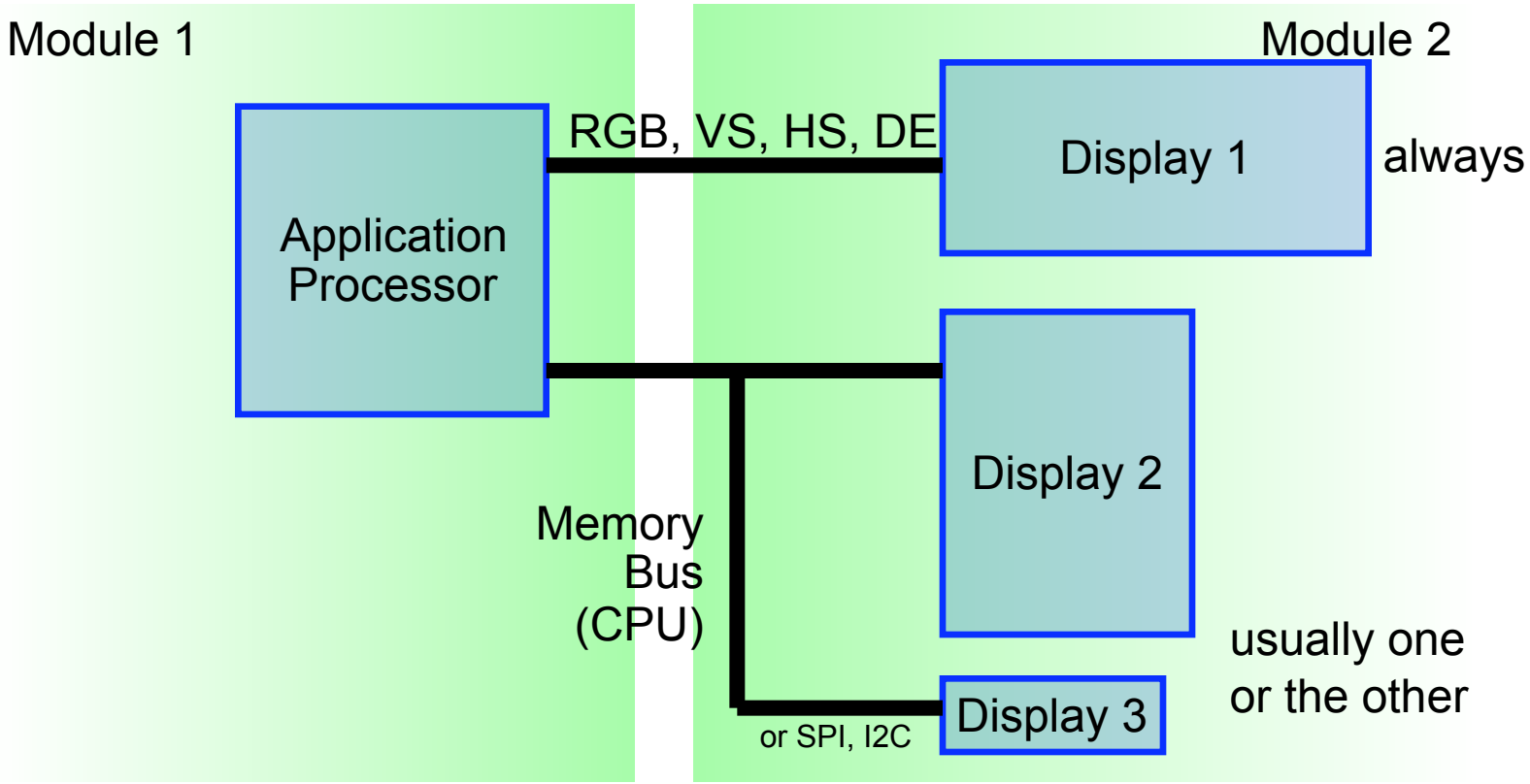
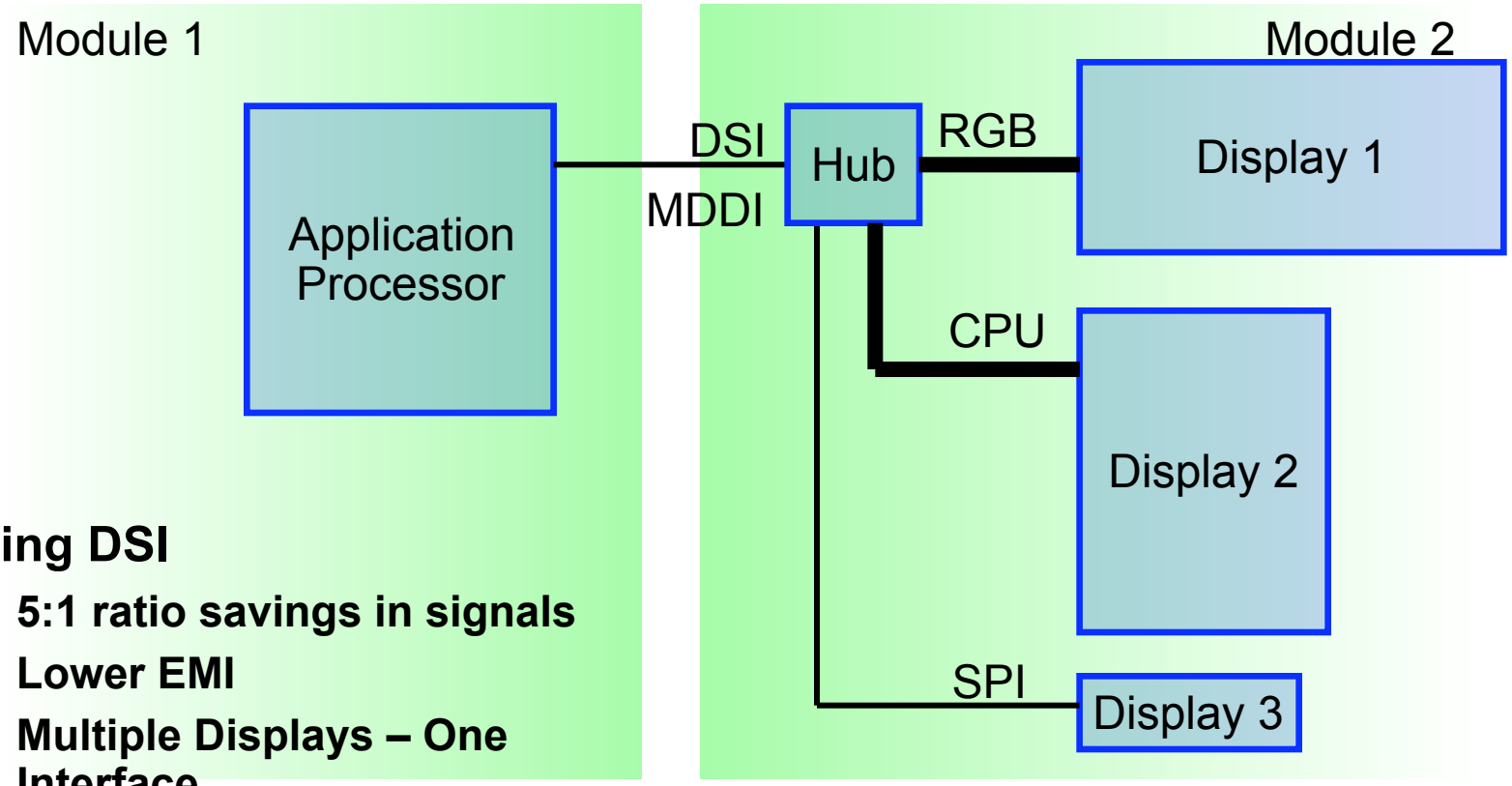
Dark ages of 2004

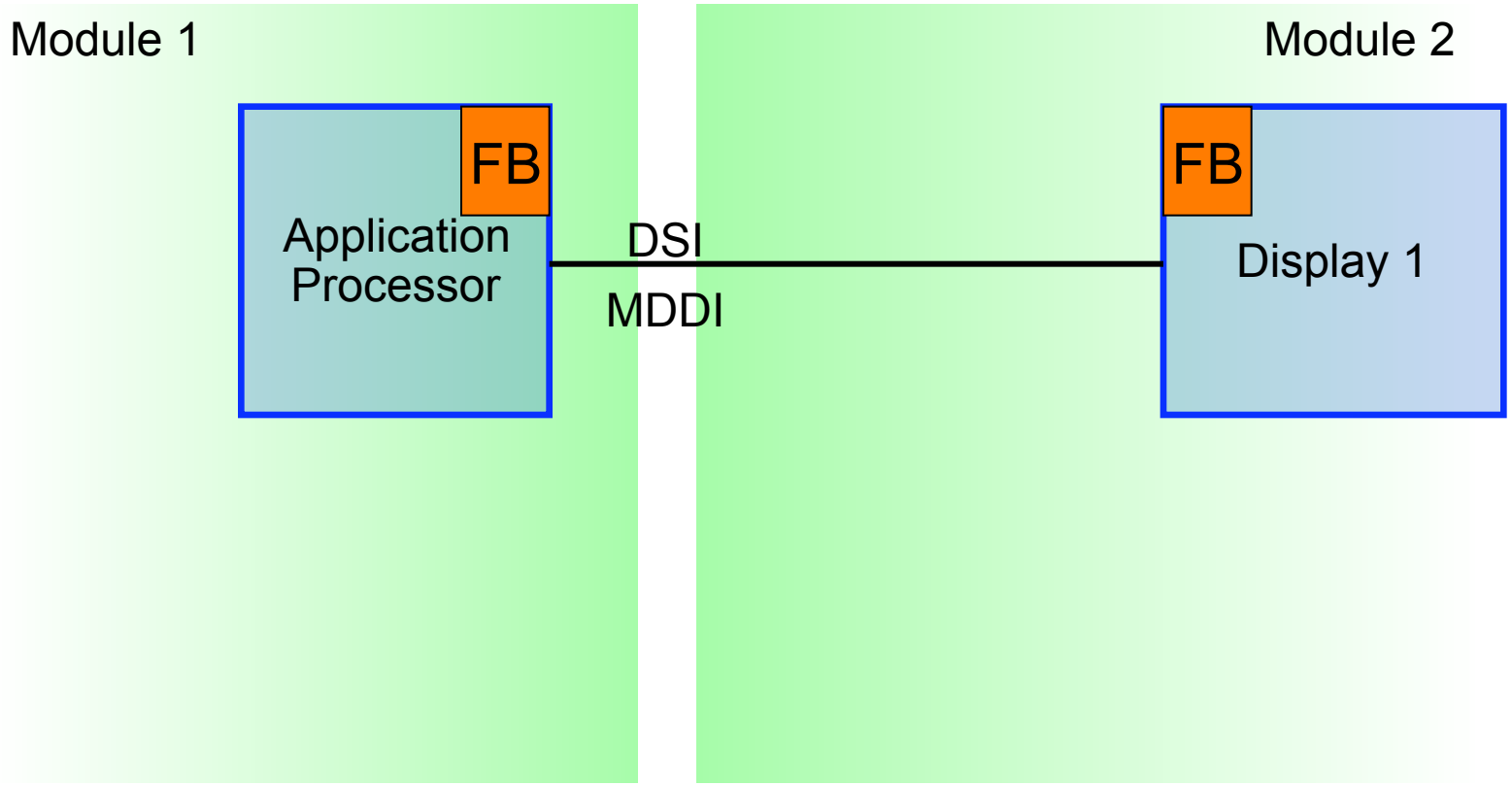


Transition Phase



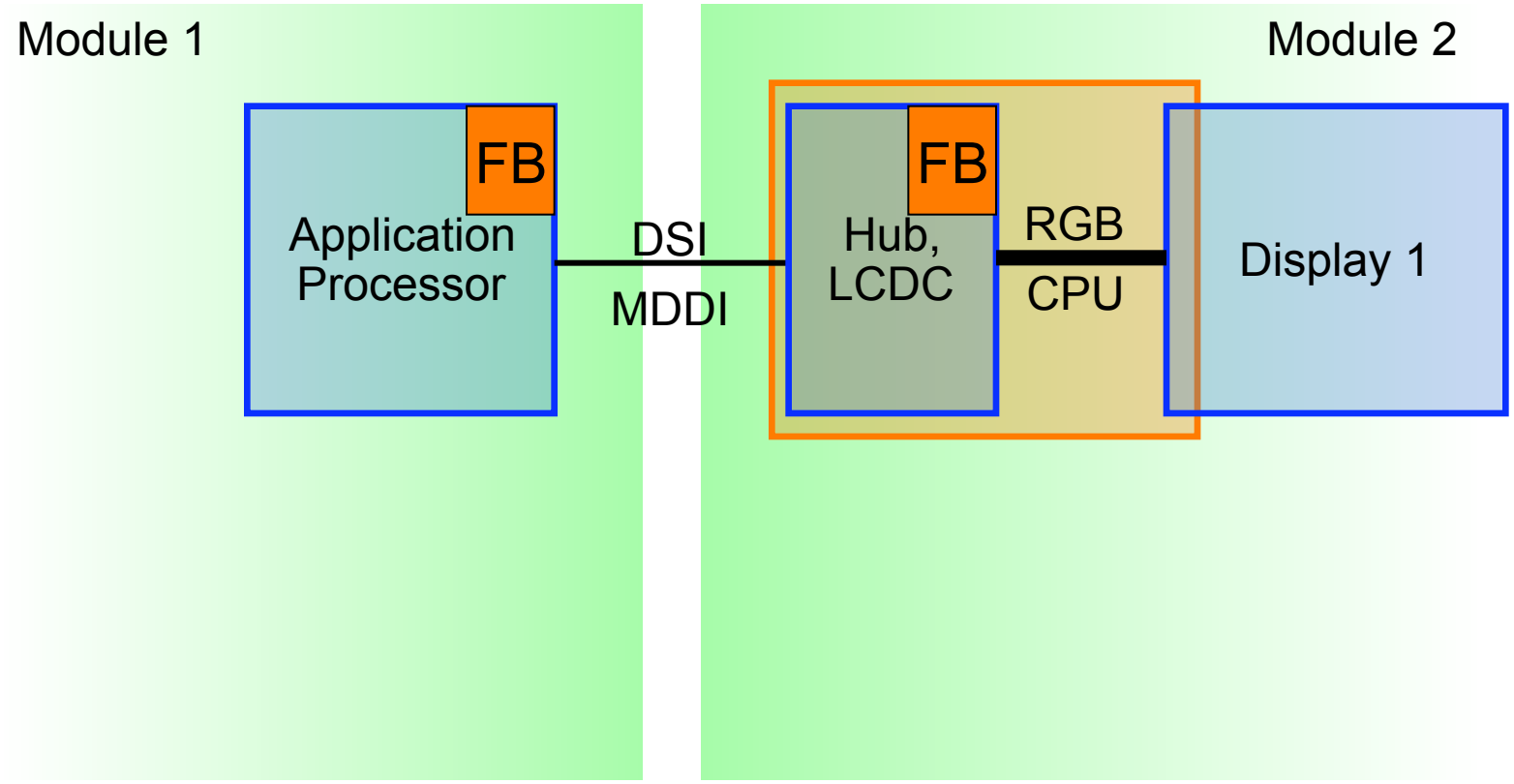
- **Using DSI**
  - **5:1 ratio savings in signals**
  - **Lower EMI**
  - **Multiple Displays – One Interface**
- **Using MDDI, additionally**
  - **Audio, KB, intelligent touch can be supported (mouse)**

Options on the Frame Buffer



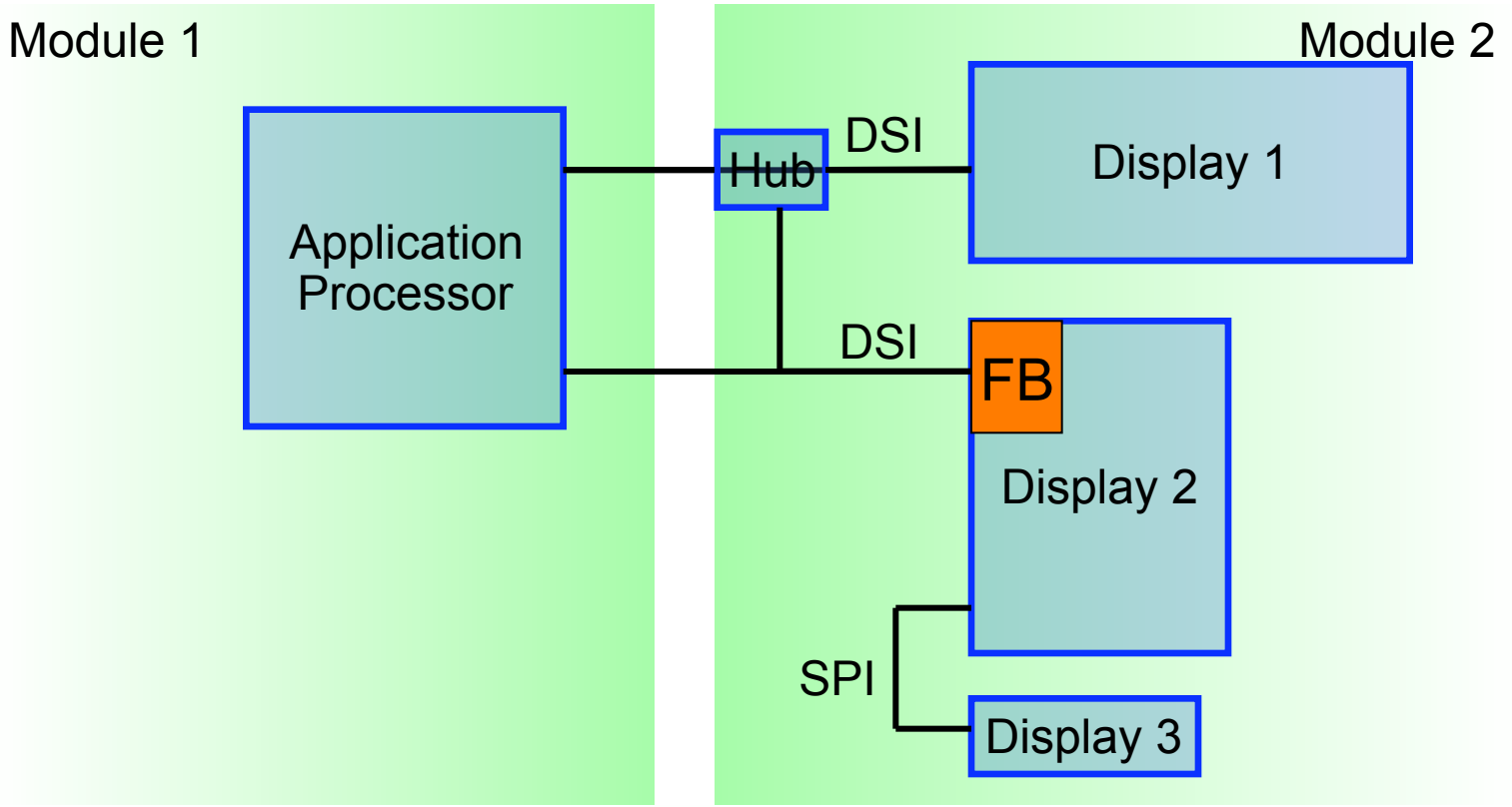
- **Opinions on the optimal locations of frame buffers continue to spark lively debate…**

Options on the Frame Buffer (2)



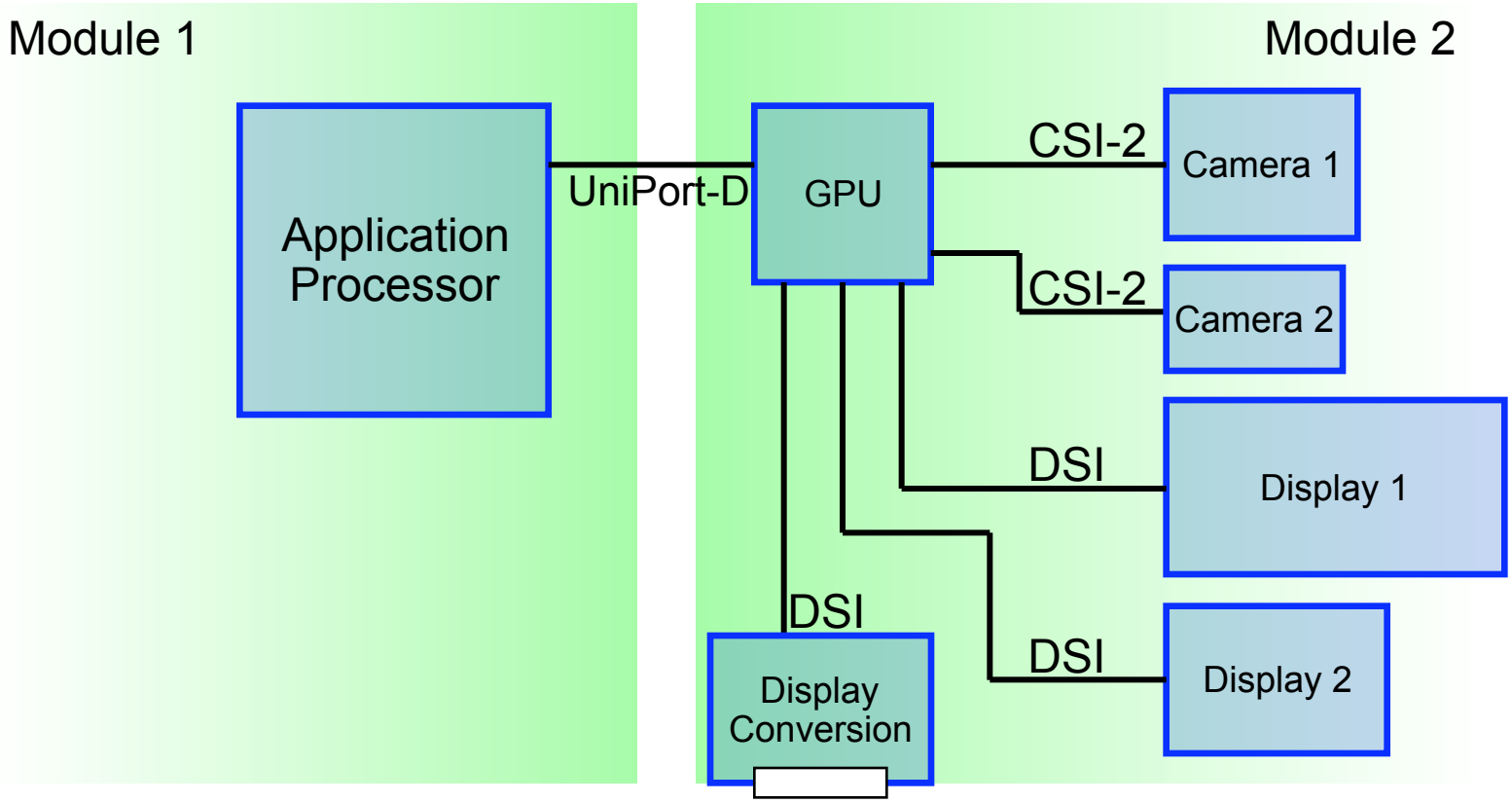
- **Cost, power consumption and supply chain are the primary motivators**

Mature serial display architectures



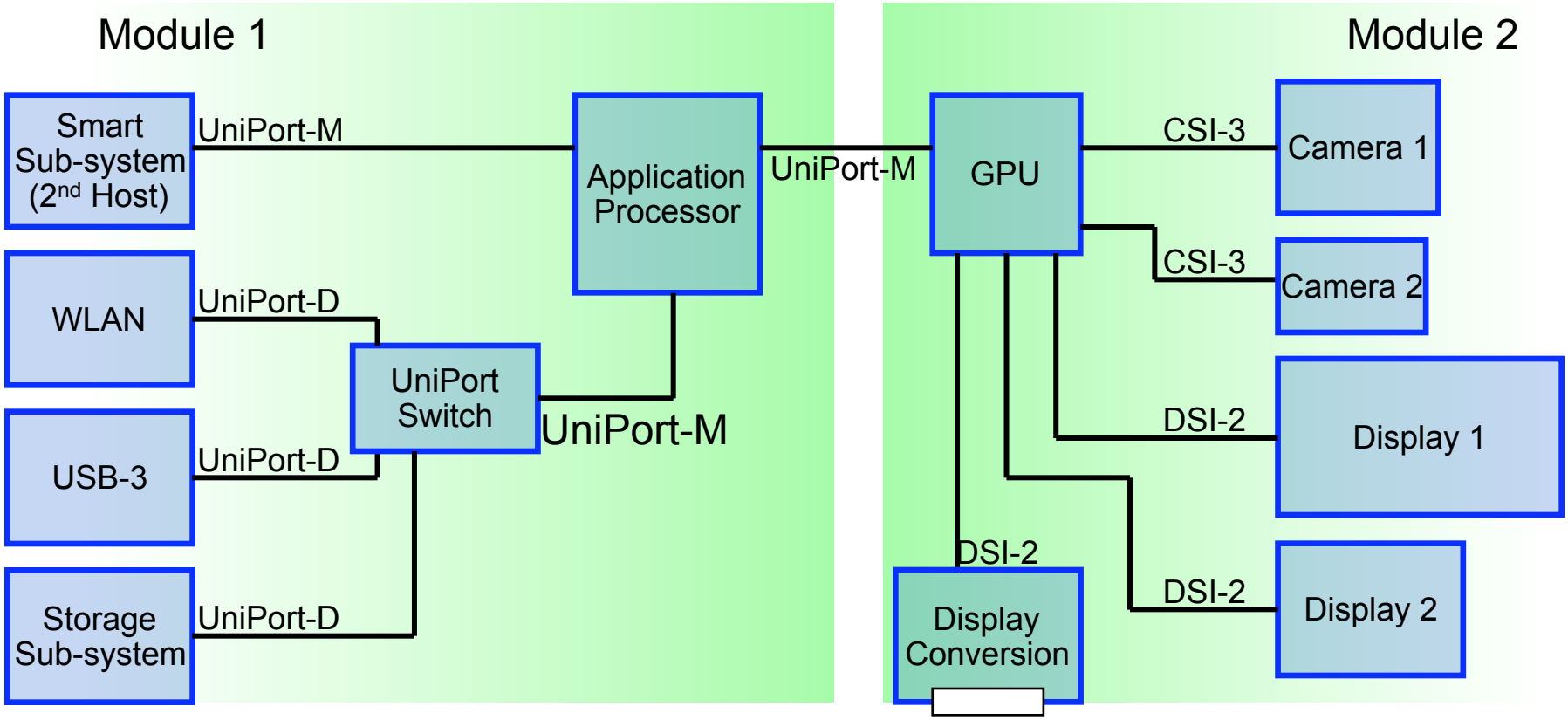
- **Many permutations of bridges and hubs during the adoption period**

UniPro with D-Phy carries heterogeneous data



- **En.wikipedia.org/wiki/Unipro**

A fully serial data architecture



- **MIPI UniPro underlies Network on Terminal Architecture (NoTA)**

Network on Terminal? Isn't it all a single chip?

- Yes – low cost "single chip" mobile terminals will continue to add functionality
- and…
- No – rapid terminal evolution requires multi-chip architectures
  - Parallel busses are no longer tractable from a cost standpoint: all but the most highly integrated die are I/O ring or "pad limited" verses being "core limited" in previous generations
  - Serial display and camera interfaces are a precursor to all high bandwidth data interfaces going serial

Thank You

Let’s continue the discussion…

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